

Description

The SP3842/3843 series high are performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference under voltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output dead time, and a latch for single pulse metering.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

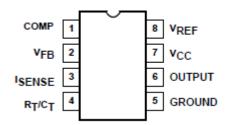
Difference between members of this series is the under-voltage lockout thresholds. The SP3842 has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters.

The corresponding thresholds for the SP3843 are 8.5 V and 7.9 V.

Features

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Under voltage Lockout
- High Current Totem Pole Output
- Under voltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

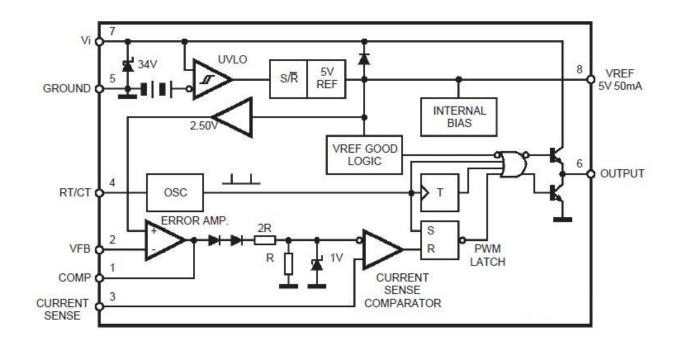
Pin Configurations (Top View)





PIN FUNCTION DESCRIPTION						
Pin No.	Function	Description				
8-Pin	Function	Description				
1	Compensatio n	This pin is the Error Amplifier output and is made available for loop compensation.				
2	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.				
3	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.				
4	Rτ/Cτ	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to Vref and capacitor C_T to ground. Operation to 500 kHz is possible.				
5	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).				
6	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.				
7	Vcc	This pin is the positive supply of the control IC.				
8	Vref	This is the reference output. It provides charging current for capacitor C_{T} through resistor $R_{T}.$				

Block Diagram





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zenger Current	(Icc+Iz)	30	mA
Output Current, Source or Sink (Note 1)	lo	1.0	А
Output Energy (Capacitive Load per Cycle)	w	5.0	<i>μ</i> J
Current Sense and Voltage Feedback Inputs	Vin	-0.3 to +5.5	V
Error Amp Output Sink Current	lo	10	mA
Power Dissipation and Thermal Characteristics			
NF Suffix, Plastic Package			
Maximum Power Dissipation @ TA=25°C	PD	862	mW
Thermal Resistance Junction to Air	Reja	145	°C/W
N Suffix, Plastic Package			
Maximum Power Dissipation @ TA=25°C	PD	1.25	W
Thermal Resistance Junction to Air	Reja	100	°C/W
Operating Junction Temperature	TJ	+150	°C
Operating Ambient Temperature	ТА		°C
SP3842/3843		0 to +70	
Storage Temperature Range	Tstg	-65 to +150	С°

ELECTRICAL CHARACTERISTICS (VCC=15 V [Note 2], RT=10 k, CT=3.3 nF, TA=TLOW

to THIGH [Note 3] unless otherwise noted)

Characteristic	SP3842/3843					
Characteristic	Symbol	Min	Тур	Мах	Unit	
REFERENCE SECTION						
Reference Output Voltage (Io=1.0 mA, TJ=25°C)	Vref	4.9	5.0	5.1	V	
Line Regulation (Vcc=12 V to 25 V)	Regline		2.0	20	mV	
Load Regulation (Io=1 mA to 20 mA)	Regload		3.0	25	mV	
Temperature Stability	Ts	—	0.2	—	mV/°C	
Total Output Variation over Line, Load, and Temperature	Vref	4.82	—	5.18	V	
Output Noise Voltage (f=10 Hz to 10 kHz, T =25°C)	Vn	_	50	—	μV	

Long Term Stability (TA=125°C for 1000 Hours)	S		5.0	_	mV
Output Short Circuit Current	lsc	-30	-85	-180	mA
OSCILLATOR SECTION					
Frequency	fosc				kHz
TJ=25°C		47	52	57	
TA=TLOW to THIGH		46		60	
Frequency Change with Voltage (Vcc=12 V to 25 V)	Δfosc/ΔV	—	0.2	1.0	%
Frequency Change with Temperature	Δfosc/ΔV	_	5.0	—	%
TA=TLOW to THIGH					
Oscillator Voltage Swing (Peak-to-Peak)	Vosc		1.6	_	V
Discharge Current (Vosc=2.0 V)	Idischg				mA
TJ=25°C		7.5	8.4	9.3	
Ta=Tlow to Thigh		7.2	—	9.5	

Notes: 1. Maximum Package power dissipation limits must be observed.

- 2. Adjust VCC above the Start-Up threshold before setting to 15 V.
- 3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible. TLOW = 0° C THIGH = $+70^{\circ}$ C
- 4. This parameter is measured at the latch trip point with VFB = 0 V.

 ΔV Output / Compensation

5. Comparator gain is defined as: AV = ΔV Current Sense Input

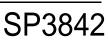
ELECTRICAL CHARACTERISTICS (VCC=15 V [Note 2], RT=10 k, CT=3.3 nF, TA=TLOW

to THIGH [Note3] unless otherwise noted)

Characteristic		SP3842/3843			
Characteristic	Symbol	Min	ТҮР	Max	Unit
ERROR AMPLIFIER SECTION					
Voltage Feedback Input (Vo=2.5 V)	Vfb	2.42	2.5	2.58	V
Input Bias Current (VFB=2.7 V)	Ів		-0.1	-2.0	μA
Open-Loop Voltage Gain (Vo=2.0 V to 4.0 V)	Avol	65	90	_	dB
Unity Gain Bandwidth (TJ=25°C)	BW	0.7	1.0	—	MHz
Power Supply Rejection Ratio (Vcc=12 V to 25 V)	PSRR	60	70	_	dB
Output Current					mA

Product specification

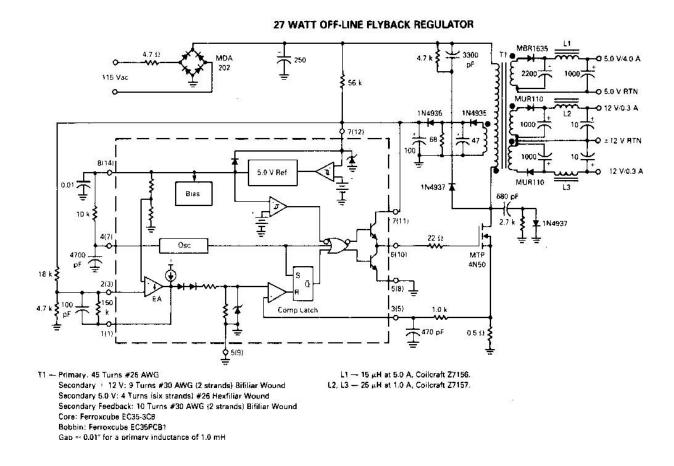




Sink (V0=1.1 V, VFB=2.7 V)	lSink	2.0	12	_	
Source (V0=5.0 V, VFB=2.3 V)	Source	-0.5	-1.0	—	
Output Voltage Swing					V
High State (R∟=15 k to ground, VFB=2.3 V)	Vон	5.0	6.2	_	
Low State (RL=15 k to Vref, VFB=2.7 V)	Vol		0.8	1.1	
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 & 5)	Av	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	Vth	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	_	70	—	dB
Vcc=12 V to 25V, Note 4					
Input Bias Current	Ів	_	-2.0	-10	μ A
Propagation Delay (Current Sense Input to Output)	tplh(in/out)	—	150	300	ns
OUTPUT SECTION					
Output Voltage					V
Low State (Isink=20 mA)	Vol	_	0.1	0.4	
(Isink=200 mA)		_	1.6	2.2	
High State (Isource=20 mA)	Vон	13	13.5	—	
(Isource=200 mA)		12	13.4		
Output Voltage with UVLO Activated Vcc=6.0 V, Isink=1.0 mA	Vol(uvlo)	_	0.1	1.1	V
Output Voltage Rise Time (C∟=1.0 nF, TJ=25°C)	tr		50	150	ns
Output Voltage Fall Time (C∟=1.0 nF, Tյ=25°C)	tf	_	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start-Up Threshold	Vth				V
SP3842/3843		14.5/7.8	16/8.4	17.5/9.0	
Minimum Operating Voltage After Turn-On	VCC(min)				V
SP3842		8.5	10	11.5	
PWM SECTION					
Duty Cycle					%
Maximum	DCmax	94	96	—	
Minimum	DCmin	_	_	0	
TOTAL DEVICE					
Power Supply Current	lcc				mA
Start-Up			0.5	1.0	
(Vcc=14 V for SP3842 /Vcc=6.5 V for SP3843)					
Operating (Note 2)		_	12	17	
Power Supply Zener Voltage (Icc=25 mA)	Vz	30	36		V



Typical Applications



Line Regulation: 5.0V	Vin=95 to 130 Vac	Δ = 50 mV or ±0.5%
±12 V		Δ = 24 mV or ±0.1%
Load Regulation: 5.0 V	Vin=115 Vac, lout= 1.0 A to 4.0 A	∆= 300 mV or ±3.0%
±12V	Vin=115 Vac, lout=100 mA to 300 mA	Δ = 60 mV or ± 0.25%
Output Ripple: 5.0 V	Vin=115 Vac	40 mVp.p
±12V		80 mVp-p
Efficiency	V _{in} =115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

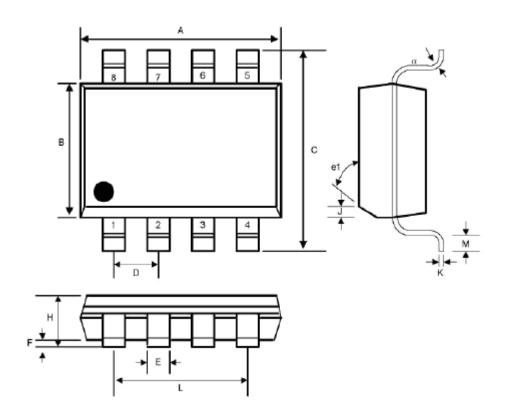


Product specification

SP3842

Package Description

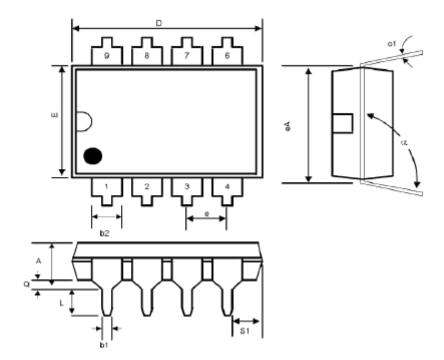
SOP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIN	NOTES	
SIMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.188	0.197	4.80	5.00	•
В	0.149	0.158	3.80	4.00	-
C	0.228	0.244	5.80	6.20	-
D	0.050 BSC		1.27 BSC		-
E	0.013	0.020	0.33	0.51	-
F	0.004	0.010	0.10	0.25	-
Н	0.053	0.069	1.35	1.75	-
J	0.011	0.019	0.28	0.48	
К	0.007	0.010	0.19	0.25	-
М	0.016	0.050	0.40	1.27	
L	0.150 REF		3.81 REF		-
e1	45°		4	5°	-
a	00 80		00	80	-







SYMBOL	INCHES		MILLIN	NOTES	
SIMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.200	-	5.08	
b1	0.014	0.023	0.36	0.58	-
b2	0.045	0.065	1.14	1.65	-
c1	0.008	0.015	0.20	0.38	-
D	0.355	0.400	9.02	10.16	-
E	0.220	0.310	5.59	7.87	-
e	0.100	BSC	2.54 BSC		-
eA	0.300	BSC	7.62	BSC	
\mathbf{L}_{i}	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	-
s1	0.005	-	0.13	-	-
α	90 ⁰	1050	90 ⁰	1050	-

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